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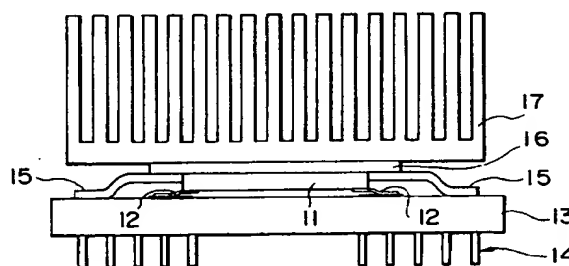
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W-8000 München 22(DE)(54) **SEMICONDUCTOR DEVICE HAVING MANY LEAD PINS.**

(57) A semiconductor device with a high package lead density such as the PGA type, allowing the density of the semiconductor device to increase by forming the leads of the semiconductor device with lead pins (14) for surface mounting arranged by the specified quantity at the outer peripheral area on the back of a package (13) where a chip (11) is mounted and lead members (22 and 41) having the predetermined function at least one of which is arranged at the internal area other than the area of the above lead pins (14).

FIG. 1A**EP 0 504 411 A1**

FILED OF THE INVENTION

The present invention relates to a semiconductor device, and particularly to a semiconductor device with a high lead density in the package.

BACKGROUND ART

FIGs. 1A and 1B are cross-sectional views of an example semiconductor device belonging to the prior art.

FIG. 1A is a cross-sectional view of a semiconductor device comprising a high-power chip and a heat sink. Bumps are formed on the face of the chip with the elements, and are bonded to TAB (Tape Automated Bonding) leads 12. This assembly is mounted onto and connected with a layer-built ceramic package. A large number of regularly spaced surface mount pins 14 project perpendicularly from an underside of this ceramic package. Power is supplied, and signals are input and output through these pins 14.

The chip 11 is encased in a metal cap 15 with its top side partially exposed. A heat sink 27 is soldered or brazed onto a top side of the chip 11, through a metal plate 16. The metal plate 16 is made of a material such as CuMo, in an attempt to make compatible the coefficients of thermal expansion of the chip 11 and of the aluminum heat sink 17.

FIG. 1B is a partial cross-sectional view of the package shown in FIG. 1A. The ceramic package 13 is constructed of ceramic layers on which is formed a pattern 13a or a power plane 13b. The pattern 13a and the power plane 13b are connected to corresponding pins 14 in the same process that the chip 11 is connected to the TAB leads 12 on which the chip is mounted by means of the bump.

The semiconductor device illustrated in FIGs. 1A and 1B is of a PGA (Pin Grid Array) type designed for increased pin population and high pin density, allowing a plurality of leads 13 to project from the underside of the package 13.

When surface mounting the semiconductor device onto the board, it is necessary to visually confirm whether has been successfully connected to the board. Since visual inspection is performed by microscope and other means, the pins 14 are provided at a periphery of the underside of the ceramic package 13, within the range where visual inspection is possible, as shown in FIGs 1A and 1B.

There is a disadvantage in this, in that visual inspection is limited to 4-6 rows of pins, prohibiting pin array placement toward the center region, and creating an area that is not usable.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a semiconductor device capable of eliminating the aforementioned disadvantage.

A more specific object of the present invention is to provide a semiconductor device that allows pins to be provided on the entire underside of a package, without having to leave any area thereof unused, and that eliminates the necessity of visual inspection.

The objects of the present invention can be achieved by a semiconductor comprising a predetermined number of surface mount lead pins provided at the periphery of the underside of a package fitted with a chip; and at least one lead part each lead part provided being assigned for a specific use, and being provided near the center region of the underside of the package, beyond the region populated with lead pins.

The objects of the present invention can also be achieved by a semiconductor device comprising a predetermined number of surface mount lead pins provided at the periphery of the underside of a package fitted with a predetermined number of chips; thin films built with interposed layers of film etched with desired patterns, for connecting the chips and the lead pins; and lead parts each assigned for a specific use, provided near the center region of the underside of the package beyond the periphery populated with the lead pins, and connected directly to the chips.

The objects of the present invention can also be achieved by a semiconductor comprising a predetermined number of lead terminals projecting from all four sides of a package fitted with a chip; and at least one lead part each provided lead part being assigned for a specific use, and provided on underside of the package.

BRIEF DESCRIPTION OF THE DRAWINGS

A more clear understanding of other objects, characteristics and utility of the present invention will be obtained by reading the explanation given below with reference to the drawings detailed below.

FIGs. 1A and 1B are cross-sectional views of an embodiment of a semiconductor device of the prior art.

FIG. 2 illustrates a first embodiment of the present invention.

FIGs. 3A to 3F illustrate a fabrication process of the embodiment of FIG. 2.

FIG. 4 illustrates a second embodiment of the present invention.

FIG. 5 illustrates a third embodiment of the present invention.

FIG. 6 illustrates a variation of the embodiment of FIG. 5.

FIGs. 7A, 7B, 8A, 8B, 9A and 9B illustrate variations of any of the first, second or third embodiment above.

FIG. 10 illustrates a fourth embodiment of the present invention.

FIGs. 11A to 11C illustrate a fifth embodiment of the present invention.

FIGs. 12A to 12D illustrate an example fabrication process of the embodiment of FIGs. 11A to 11C.

FIGs. 13A to 13I illustrate an example fabrication process of a thin film such as the one shown in FIG. 12A.

FIGs. 14A and 14B illustrate another example fabrication process of the embodiment of FIGs. 11A to FIG. 11C.

FIG. 15 illustrates a sixth embodiment of the present invention.

FIGs. 16A and 16B illustrates a seventh embodiment of the present invention.

FIGs. 17A and 17B illustrate a variation of the embodiment of FIG. 16.

BEST MODE OF CARRYING OUT THE INVENTION

FIG. 2 illustrates a first embodiment of the present invention. The semiconductor 11 of FIG. 2 is, for example, a high-power chip and is provided with a heat sink 17, a metal cap 15, and a metal plate 16 between the heat sink and the metal cap. Bumps are formed on the face of the chip 11 with the elements, and are bonded to TAB leads 12. Bumps can alternatively be formed on the TAB leads 12. The assembly is mounted onto and connected with a ceramic package 13.

Regularly spaced lead pins 14 (for signals for example), are provided projecting perpendicularly from the underside of the package, in 5 rows for example, at the periphery of the ceramic package. These lead pins 14 are surface mount lead pins, and are connected to the pattern formed in respective layers within the multi-layer ceramic package 13 (see FIG. 1B).

Cylindrical lead pins 22, are provided, as lead parts each assigned for a specific use, toward the interior 21 of the underside of the ceramic package 13, beyond the region populated with the lead pins 14, in 4 groups of 9 pins each, for example (see FIG. 4). Cylindrical lead pins 22 each assigned for a specific use include, for example, power lead pins 22a and 22c or ground lead pins 22b and 22d. They are larger than the lead pins 14 in thickness, and are formed for surface mount. Their use makes power circuit connection easy.

The lead pins 22 need not be cylindrical in

shape, but can be of any shape including octagonal columns or hexagonal columns. The lead pins 22 are made of the same material as the lead pins 14 and are plated with gold, for example. The reason for forming the lead pins 22 thicker than the lead pins 14 is to ensure, in the present invention, that electric connection is established by eliminating a slight displacement that occurs in prior art when mounting a semiconductor device onto the board. Accordingly, the lead pins 22 are more sparsely spaced than the lead pins 14.

While in the above embodiment a plurality of lead pins 22 are provided, providing at least one lead pin 22 ensures performance.

When a semiconductor device as the one described in the above embodiment is mounted onto a board, electric connection of 5 rows of lead pins 14 with the board is confirmable visually. The necessity of visual inspection of the lead pins 22 provided in the interior 21 is eliminated since the connection of one pin alone among 9 ensures performance.

This way, it is possible to avoid leaving any unused room on the entire underside of the ceramic package 13, in providing pins. It also becomes possible to assign the lead pins 14, provided in the periphery, for signal use only, thus allowing provision of a denser array useful for decreasing capacitance and resistance, improving high-frequency properties, and increasing the chance of down-scaling the entire composite.

FIGs. 3A to 3F illustrate an example fabrication process of the embodiment of FIG. 2. First, a TAB film 32 is prepared on which TAB leads 12 are formed corresponding to a plurality of pads 31 placed on the chip 1 (FIGs. 3A, and 3B). Bumps are formed either on the pads 31 of the chip 11 or on an end of each TAB lead 12, or on both. The chip 11 is joined with the TAB leads 12 by bonding. Then the TAB leads 12 are cut from the TAB film 32 (FIG. 3C).

The ceramic package 13 is formed by building layers of ceramic on which specific patterns 33 have been formed. The lead pins 14 and the lead pins 22 project from the underside of the package as shown in FIG. 2 (FIG. 3D). The edge of the pattern on the uppermost layer in the ceramic package and the edge of the TAB leads 12 joined with the chip 11 are bonded by means of face down bonding (FIG. 3D).

A metal cap 15 is then soldered or brazed above the uppermost layer of the ceramic package 13 in such a way as to encase the chip 11 (FIG. 3E). A metal plate 16 is soldered or brazed onto this metal cap 15 and the chip 11, then a heat sink 17 is soldered or brazed onto the metal plate 16 (FIG. 3F). The metal cap 15, the metal plate 16 and the heat sink 17 may be joined together in ad-

vance.

FIG. 4 illustrates a second embodiment of the present invention. A semiconductor device in FIG. 4 is shown mounted on a board 42. The semiconductor herein is essentially the same as in FIG. 2 except that it is provided with lead pins 41 (power pins 41a and ground pins 41b, specifically) obtained by extending the lead pins 22 of the previous embodiment so that they are longer than the lead pins 14 at the periphery. In this case, corresponding positions on the board for mounting of the composite, are provided with through-holes 44a to allow the lead pins 41 to go through. In other words, the lead pins 14 at the periphery are surface mounted, while the lead pins 41 are mounted by soldering, for example by allowing them to go through the through-holes 42a.

The above construction allows the lead pins 41 to serve as an insertion guide into the through-holes 42a, facilitating alignment during surface mount. Direct connection of the lead pins 41 with the board 42 decreases the inductance component.

Connection of the lead pins 41 with the board 42 can easily be inspected visually by looking at underside of the board 42 since the lead pins 41 go through the board 42.

FIG. 5 is a bottom view of a third embodiment of the present invention. In a semiconductor device shown in FIG. 5, the lead pins 22 (41) such as those shown in FIGs. 2 and 4 are provided in such a manner that they encompass terminal(s) 51 assigned for use as, for example, clock pins in semiconductor circuits. It is possible thus to attain increased stability in the operation of the device due to encompassing the terminal(s) 51 with the lead pins 22 (41), which are not susceptible to fluctuation in potential as they are assigned as power and signal pins, thus preventing the noise.

The terminal(s) 51 can ensure a secure mounting, by eliminating displacement that occurs when mounting the composite on the board, by forming the terminal(s) so as to be thicker than the lead pins 14 as in the case of the lead pins 22 (41).

FIG. 6 illustrates a variation of the embodiment of FIG. 5. The terminal(s) 51 in FIG. 6 are formed longer than the lead pins 22. In this case, through-holes 42a are drilled on a board 42 for mounting of the composite, and the terminals 51 come through the through-holes 42a to be soldered on the board. Here, the terminals 51 can serve as a guide in mounting. Alternatively, the lead pins here can be like the lead pins 41 in FIG. 4, which are longer than the lead pins 14. They can also go through the board 42 and be fixed. By using these methods, visual inspection of the solder joint is possible from the underside of the board.

FIGs. 7 to 9 illustrate variations of the above embodiment.

FIG. 7A is a cross-sectional view, and FIG. 7B is a partial bottom view. (Note that the chip 11 on upper side, the heat sink 17, etc. will be left out of the diagrams hereinafter through FIG. 9B). The semiconductor device in FIGs. 7A and 7B is fabricated in such a way that square-shaped one or more lead parts 71 that look like a block are provided toward the interior 21 on the underside of the package 13 beyond the region populated with the lead pins 41. These lead parts 71 can be assigned as power pins in the semiconductor circuit, for example. With this semiconductor it is possible to achieve a wide contact area with the board when mounting the composite, and to have the composite soldered to the corresponding pattern on the board with accuracy, even when displacement occurs. This way, the process of visual inspection of connections can be eliminated.

FIG. 8A is a partial cross-sectional view, and FIG. 8B is a partial bottom view. The semiconductor device shown in FIGs. 8A and 8B is fabricated in such a way that cylindrical block-shaped lead parts 81 are provided in place of the lead parts 71 shown in FIGs. 7A and 7B, for the same use. These lead parts 81 are spaced more sparsely than the lead pins 14 and are surface mounted as in FIGs. 7A and 7B. Accordingly, because the lead parts 81 are block-shaped, a more secure connection with the board is achieved, and the process of visual inspection can be eliminated.

FIG. 9A is a partial cross-sectional view, and FIG. 9B is a partial bottom view. The semiconductor device shown in FIGs. 9A and 9B is fabricated in such a way that lead parts having L-plate shape, are provided in place of the lead parts 71 or 81 above. The usefulness of this configuration when the composite is mounted on the board is the same as that of the configuration with the lead parts 71 or 81.

FIG. 10 illustrates a fourth embodiment of the present invention. The semiconductor device shown in FIG. 10 is fabricated in such a way that a high-power chip 111 is mounted on a depression 113a formed on a metal base 113a. A thin film 112 is positioned on the same plane as the upper surface of the chip. The chip is joined to the thin film 112 on both ends of the face with the elements, through TAB leads 114, with the use of bumps. These thin films 112a and 112b are TABs produced by layering thin films (made of polyimide, etc.) etched with fine patterns, and are supplied with signal pads (described later) for connection with the TAB leads 114 and pins to be described later. That is, this thin film 112 acts to disperse the layout of the lead pins connected thereto. The metal base 113 on which the chip 111 and other things are mounted is soldered or brazed to an underside of a heat sink 115 formed of a

material such as aluminum. This metal base 113 is formed of a material such as CuMo, and is designed for making compatible the coefficients of thermal expansion between the chip 111 and the heat sink 115 as they are bonded together.

The package 116 is fabricated in such a way that it allows signal lead pins 14 to project at the periphery of its underside; it also allows lead pins 22, each assigned for a specific use, to project from a region toward the interior 21 of the underside, and is provided with a depression (PGA type). The signal lead pins 14 project perpendicularly in 4 to 6 rows and are spaced regularly, so that they can be visually inspected when mounted on the board. The package 116 comprises layers of ceramic etched with a power plane 117, which is a power supply pattern. A predetermined number of lead pins 22 connected with the power plane 117 is provided in the interior 21 on the underside of the package 116. These lead pins 22 are formed thick enough to make them differentiable from the signal lead pins 14, and to eliminate displacement while mounting the composite onto the board. They are used, for example, as power pins, or as clock pins sealed by the power pins.

The package 116 is then fitted to the metal base 113 with adhesive, for example. The signal lead pins 14 are electrically connected with signal pads on the thin film 112 through contact pins 118a placed in a pressurized contact with the pins. Some of the lead pins 22 and power supply pads formed on the chip 111 are electrically connected through contact pins 118b.

A semiconductor device such as this can be made thin since it requires only the power plane 117 inside the package 116. Use compatible with semiconductor devices having chips of other functions is also possible. Direct contact of the power lead pins 22 with the chip 2 assures low impedance because an intermediate conductor pattern is eliminated. Moreover, even if the metal base 113 is taken away from the package 116 it is restorable since the connections among the lead pins 14, the lead pins 22, the chip 111, and the thin film 112 are achieved by pressurized contact only, with the use of the contact pins 118a and 118b. This makes failure analysis of the device easier, and improves fabrication yield. Moreover, since a group of inner power leads 12 are provided in the interior 14, thus increasing the likelihood that electric contact is established, the process of visual inspection of the connection can be eliminated when mounting such a semiconductor device onto the board.

While FIG. 11 shows the electric connection of the lead pins 14a and 22 with the thin film 112 achieved by means of the contact pins 118a and 118b, use of bumps instead can make the device smaller in proportion to the dimensions of the con-

tact pins 118a and 118b.

Direct connection of some of the lead pins 12 with the chip 111 in this embodiment may be replaced by another connection means, wherein the pins are connected with the chip 111 through the thin film 112 by means such as TAB leads, for example. In this manner the structure is simplified and crosstalk arising from the signal lead pins 14 is prevented.

The lead pins 22 can also serve as a guide when mounting the composite if they are made longer than the lead pins 14, as shown in FIG. 4.

FIGs. 11A to 11C illustrate a fifth embodiment of the present invention. In this embodiment, the contact pins 118a and 118b in FIG. 10, used for connections among the lead pins 14, 22, the film 112 and the chip 111, are replaced by bumps. Accordingly, FIGs. 11A to 11C are partial cross-sectional views showing an area in which bumps are formed. Configuration other than as concerns the bumps remains the same as in FIG. 10.

FIG. 11A is a part of a top cross-sectional view, and FIG. 11B is a part of its side cross-sectional view showing a relationship between a chip and a thin film. In FIGs. 11A and 11B, a chip 111 is mounted onto a metal base 113. In the periphery of the chip, the thin film is positioned on the same plane as the topside of the chip. A signal pattern 119a, for example, and a power pattern 119b, for example, are formed on the thin film 112, each layer being connected by through-holes.

The topmost pattern 119a of the thin film 12 is bumped (120) at one end thereof, while the other end is connected to a pad 121 of the chip 111 via a TAB lead 114. Around the thin film 112 is formed a seal pattern 122. The thin film 112 here differs from the thin film 112 in FIG. 10 in that it comprises a bump.

FIG. 11C illustrates a relationship between the thin film and the lead pins. FIG. 11C shows that the bump 120 formed on the pattern 119a of FIGs. 11A and 11B, and the bump 120 formed on the pattern 122 provided on the surface of the package 116 are completely joined by pressure. This happens between each pattern 119a and a corresponding lead pin 14, so as to establish an electrical connection.

FIGs. 12A to 12D illustrate an example fabrication of the device of FIGs. 11A to 11C. First, FIG. 12A shows that a thin film 112 having an opening 112a that corresponds to a depression 113a is formed around the depression 113a provided in a metal base 113 attached to a heat sink 15. FIG. 12B shows a chip 111 mounted onto the depression 113a of the metal base 113. FIG. 12C shows that the chip 111 and the thin film 112 are connected via TAB leads 114, as shown in FIGs. 11A and 11B. Bumps 120 are formed on the interface

between the chip 111 and the thin film 112. FIG. 12D shows that the patterned portion of a package 116 formed so as to connect to lead pins 14 and 22 projecting from the surface of the package 116, is bumped (120). Connection is established by pressure joining the bumps 120 against the corresponding bumps 120 formed on the chip 111 and the thin film 112 so that the connection is complete. The package 116 and the periphery of the metal base 113 are then sealed by soldering.

The semiconductor device of the prior art shown in the FIG. 1 has a disadvantage in that it is difficult to judge whether such parts as the chip and the metal base are firmly united. It also leaves a possibility of solder leakage between the chip and the metal base. With the semiconductors fabricated in the process of the present invention, on the other hand, it is sufficient to have the periphery of the package 116 and the metal base 113 united; inspection is easy.

The power lead pins 22 can be alternatively connected via the thin film 112 by providing a pattern on the package 116, thus eliminating a direct connection with the chip 111. In this way crosstalk can be avoided just as surely as in the above mentioned manner.

FIGs. 13A to 13I illustrate an example process for forming the thin film such as the one shown in the FIG. 12A. First, a metal layer 131 is formed on a metal base (FIG. 13A) by a method such as evaporation (FIG. 13B). The metal layer 131 is treated with photoresist 132 (FIG. 13C), and a pattern 132a is formed after lithography and a development process (FIG. 13D). The metal layer 131 is then etched to create a pattern 131a (FIG. 13E). The photoresist pattern 132a is then removed (FIG. 13F).

Photosensitive polyimide 133 is then spin coated onto the metal pattern 131a (FIG. 13G), which is exposed after the lithography and development process. After the polyimide 133 is hardened by heating (FIG. 13H), metal layer 134 is formed by a process such as evaporation, and is connected with the metal pattern 131a below (FIG. 13I).

A repetition of these processes in building 4 or 5 layers forms a thin film 112.

Although it is not shown in the figure, an opening 112a of FIG. 12A is formed in each layer formed in the above process.

FIGs. 14A and 14B illustrate another example fabrication process of device of FIGs. 11A to 11C. FIG. 14A shows a process in which the opening 112a of the FIG. 12A is not formed, but wherein a thin film 112 is formed by building 4 or 5 layers of patterned polyimide on a metal base 113 (see FIGs. 13A to 13I). A chip 111 is mounted onto this thin film 112, and the chip 111 and the pattern on the thin film 112 are bonded by a wire 141. Bumps

120 are formed on one end of a pattern 119a on the thin film 112 and on a pad 121 on the chip 111.

FIG. 14B shows a pattern 142 formed on a layer-built package 116 comprising lead pins 14 and 22 projecting from the underside of the package. Bumps 120 are formed on the end of the pattern. Pressure joining the bumps 120 on the chip 111 and the thin film 112 to the corresponding bumps 120 on the pattern 142 unites the composites.

FIG. 15 illustrates a sixth embodiment of the present invention. A semiconductor device shown in FIG. 15 is a side cross-sectional view of a multi-chip embodiment. FIG. 15 shows chips 111 and 111A connected through TAB leads 114A. Other configurations remain the same as the semiconductor device of FIG. 10. This exemplifies a multi-chip embodiment, which was impossible in the prior art.

While FIG. 15 shows the chips 111 and 111A connected through the TAB leads 114A, this arrangement can be replaced by a configuration where a thin film comprising patterned polyimide layers is interposed between the chips 111 and 111A so that TAB leads can connect them.

Connection between the chips 111 and 111A, and the thin film 112 can be accomplished by wire-bonding as illustrated in FIG. 14 and 14B.

In the fifth and sixth embodiments above, the lead pins 22 are described as having the role, in surface mounting, as in the embodiment of FIG. 2. Accordingly, the function of these lead pins 22 is the same as that described in FIG. 2. When extended to be as those shown in FIG. 4, these lead pins function in the same way as in the embodiment of FIG. 4. When terminal(s) 51 are provided as shown in FIGs. 5 and 6, the terminals have the same function as in FIGs. 5 and 6. The lead pins 22 may alternatively be formed into shapes as shown in any of FIGs 7 to 9.

While the use of ceramic package was assumed in the first to sixth embodiments above, a package formed with such resin as epoxy, or metal, also assures performance. Further, these embodiments have the same utility with semiconductor devices fitted with a chip not needing a heat sink.

FIGs. 16A and 16B illustrate a seventh embodiment of the present invention. While the use of a PGA type semiconductor device was assumed in any of the first to sixth embodiments above, this embodiment comprises a QFP (Quad Flat Package) type semiconductor device.

In the semiconductor device shown in FIGs. 16A and 16B, lead pins 162 project from all four sides of a package (ceramic or resin mold) 161, and are shaped like an L-plates for the purpose of surface mount. Moreover, at least one lead part

163 project from the underside of the package. Provided lead part 163 can be of any form including those of the lead pins 22, 41, and the lead parts 71, 81, 91 above. Clock terminal(s) 51 are provided, when needed. With this configuration, the vacant region of a QFP type package can be utilized effectively.

FIGs 17A and 17B illustrate a variation of the embodiments of FIG. 16. In a QFP type semiconductor shown in FIG. 17, lead part(s) 171 with the shape of an L-plates are provided on the underside of a package 161.

Thus, any of the first to seventh embodiments show that it is possible to provide pins effectively by providing lead parts, each assigned for specific use, in the otherwise unoccupied region on the underside of the package, and to ensure the connection is established when mounting the composite onto the board, and to eliminate the process of visual inspection. The present invention also makes layer-building of the package easy and facilitates down-scaling. Providing power lead parts on the underside of the package ensures a high density of signal lead pins, and increases the capacity of a semiconductor integrated circuit.

POSSIBLE APPLICATION IN INDUSTRY

As explained above, the present invention allows effective pin array placement on the entire underside of a package, and eliminates the process of visual inspection when mounting the composite onto the board, thus realizing high density and greater capacity of the semiconductor device.

The present invention can find applications in high-density semiconductor devices including a PGA type and a QFP type.

Claims

1. A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (13) fitted with a chip (11); and
 - a plurality of surface mount lead members (22), each assigned for a specific use and provided near a center region of the underside of said package (13) beyond the region populated with said lead pins (14),
 - at least two lead pins (22) for the same use being included in said surface mount lead members (22).
2. A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (13) fitted with a chip

(11); and

at least one lead member (41), each assigned for a specific use, said lead member (41) being longer than said lead pins (14) and provided near a center region on the underside of said package (13) beyond the region populated with said lead pins (14).

3. A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (116) fitted with a predetermined number of chips (11); and
 - a thin film (112) built with layers of patterned films, and interposed between the chip (41) and the lead pins (14), for connecting said chip (111) and said lead pins (14); and
 - at least one lead member (22, 41), each assigned for a specific use, connected to said chip (111) without the interposition of said wiring pattern on said thin film (112) and provided near a center region beyond the region populated with said lead pins (14).
4. A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (116) fitted with a predetermined number of chips (111); and
 - a thin film (112) built with layers of patterned films, said layers being interposed for connecting said chip (111) and said lead pins (14); and
 - at least one lead member (22, 41), each assigned for a specific use, connected to said chip (111) through said interposed thin film (112) and provided near the center beyond the region populated with said lead pins (14).
5. A semiconductor device as claimed in claim 3 or claim 4, wherein a plurality of chips (111, 111A) are mounted, and a connection between said chips (111, 111A) is accomplished by interposing said thin film (112) between the chips.
6. A semiconductor device comprising:
 - a predetermined number of lead terminals (162) projecting from all four sides of a package (161) fitted with a chip; and
 - a plurality of surface mount lead members (163), each assigned for a specific use and provided on an underside of said package (161),
 - at least two lead members (163) for the same use being included in said surface mount lead members.

7. A semiconductor device comprising:
 - a predetermined number of lead terminals (162) projecting from all sides of a package (161) fitted with a chip (111); and
 - at least one member (163), each assigned for a specific use and provided on an underside of said package (161),
 - wherein said lead members (163) project further from the underside of the package (161) than said lead terminals.
8. A semiconductor device as claimed in any of claims 1 to 7, wherein said lead members (22, 41, 163) comprise a plurality of groups of lead members having a plurality of functions,
 - wherein each of the groups of lead members (22, 41, 163) has one specific function, and consists of a plurality of lead members, and the neighboring lead members within each group are more sparsely populated than the lead members found in any other configuration.
9. A semiconductor device as claimed in any of claims 1 to 8, wherein said lead members (22, 41, 163) serve as a power supply system in a semiconductor circuit.
10. A semiconductor device as claimed in any of claims 1 to 9, wherein said lead members (22, 41, 163) are thicker than said lead pins (14) having a column shape.
11. A semiconductor device as claimed in claim 2 or claim 7, wherein said lead members (22, 41, 163) having a column shape, longer than said lead pins (14), serve as guides pin when mounting the composite onto said board (42).
12. A semiconductor device as claimed in any of claims 1 to 9, wherein said lead members (22, 41, 163) comprise a block shape (71, 81).
13. A semiconductor device as claimed in any of claims 1 to 9, wherein said lead members (22, 41, 163) comprise an L-plate plate (91, 171).
14. A semiconductor device as claimed in any of claims 1 to 13, comprising terminals (51) each assigned for a specific use, and encompassed by said lead members (22, 41, 163).
15. A semiconductor device as claimed in claim 14, wherein said terminals (51) are longer than said lead pins (14), so as to go through the board and be fixed onto it when mounting the composite onto the board.

16. A semiconductor device as claimed in claim 15, wherein said terminals (51), longer than said lead pins (14), serve as a guide when mounting the composite onto said board (42).
17. A semiconductor device as claimed in any of claims 14 to 16, wherein said terminals (51) serve as clock terminals in the semiconductor circuit.

Amended claims

Claims 1,3,4 and 6 are amended, and claims 2,5 and 7 - 17 are not amended.

1. (amended) A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (13) fitted with a chip (11); and
 - a plurality of surface mount lead members (22), each assigned for a specific use, and provided near a center region of the underside of said package, beyond the region populated with said lead pins (14),
 - at least two lead members (22) for the same use being included in said surface mount lead members (22), and said function being fulfilled by connecting any of said lead members (22) to conductive members on the board on which the composite is to be mounted.
2. A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (13) fitted with a chip (11); and
 - at least one lead member (41), each assigned for a specific use, said lead part (41) being longer than said lead pins (14) and provided near a center region on the underside of said package (13) beyond the region populated with said lead pins (14).
3. (amended) A semiconductor device comprising:
 - a predetermined number of surface mount lead pins (14) each assigned for a specific use and provided at a periphery of an underside of a package (16) fitted with a predetermined number of chips (11);
 - thin films (112) built with layers of films etched with desired wiring patterns and interposed between said chip (11) and said lead pins (14) for connecting said chip (111) and said lead pins (14), and
 - at least one lead member (22, 41) each

assigned for a specific use, connected to said chip (111) without the interposition of said wiring patterns on said thin films (112) and provided near the center beyond the region populated with said lead pins (14).

5

claims 1 to 7, wherein said lead members (22, 41, 163)

4. (amended) A semiconductor device comprising:

a predetermined number of surface mount lead pins (14) provided at a periphery of an underside of a package (16) fitted with a predetermined number of chips (11);

10

thin films (112) built with layers of films etched with desired wiring patterns and interposed between said chip (11) and said lead pins (14) for connecting said chip (111) and said lead pins (14); and

15

at least one lead member (22, 41) each assigned for a specific use and provided near a center beyond an region populated with said lead pins (14), and connected to said chip (111) through the interposition of said thin films (112).

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5. A semiconductor device as claimed in claim 3 or claim 4, wherein a plurality of said chips (111, 111A) are provided and a connection between said chips is accomplished through the interposition of said thin film (112).

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6. (amended) A semiconductor device comprising:

a predetermined number of lead terminals (162) projecting from all four sides of a package fitted with a chip; and

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a plurality of surface mount lead members (163) each assigned for a specific use and provided on an underside of said package (161),

at least two lead members (163) being provided for the same function, and said function being fulfilled by connecting any of said lead members (163) with a conductive member on a board on which the composite is to be mounted.

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7. A semiconductor device comprising:

a predetermined number of lead terminals (162) projecting from all four sides of a package (161) fitted with a chip; and

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at least one lead member (163) each assigned for a specific use and provided on an underside of said package (161),

wherein, said lead members (163) project further from the underside of said package (161) than said lead terminals.

55

8. A semiconductor device as claimed in any of

FIG. 1A

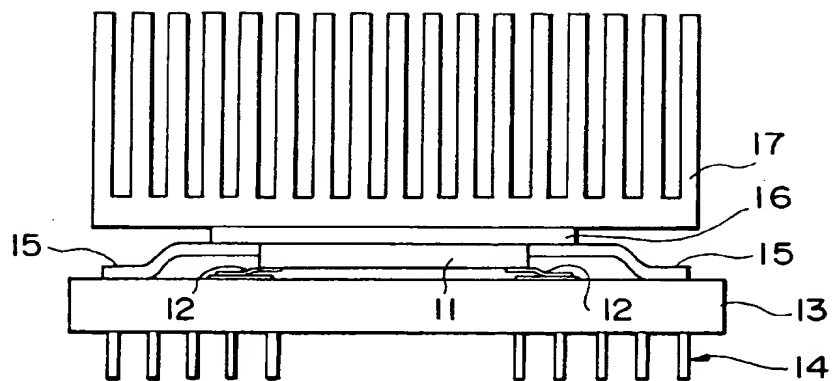


FIG. 1B

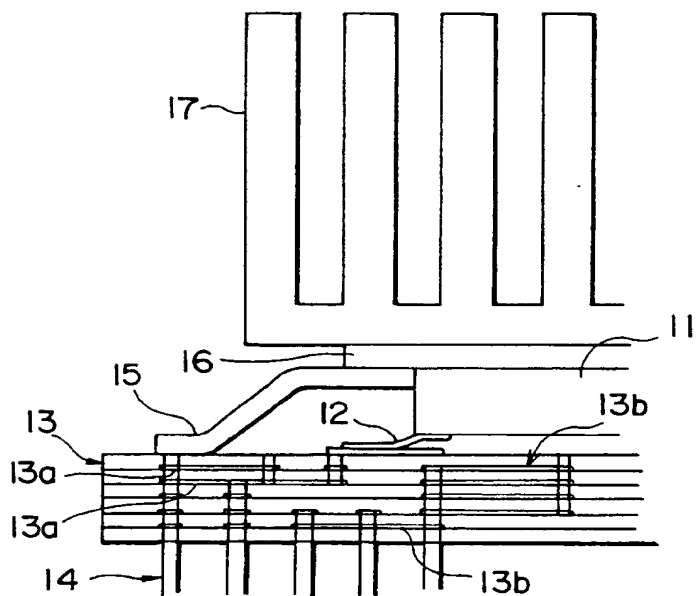


FIG. 2

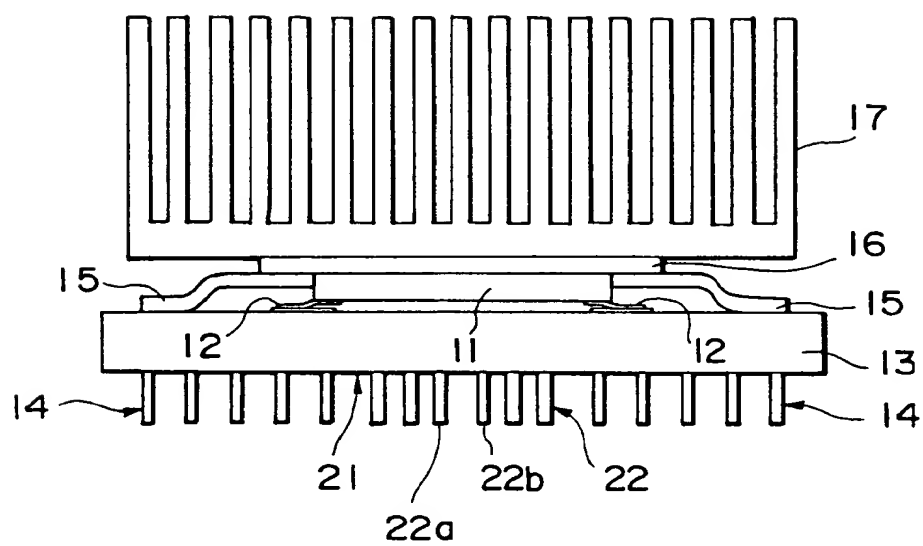


FIG. 3A

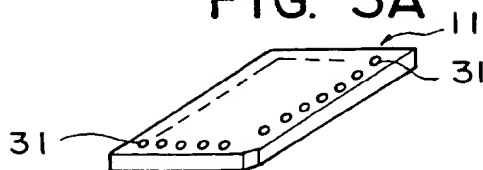


FIG. 3B

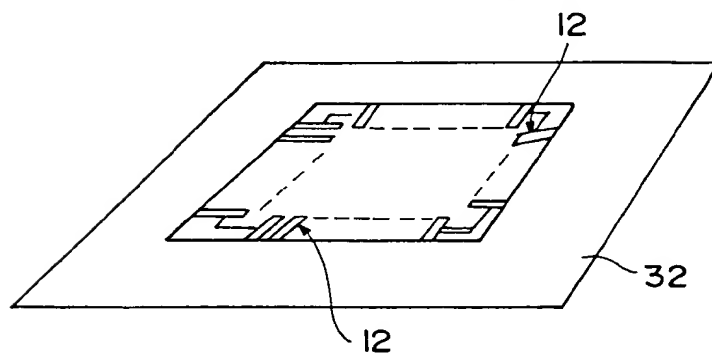


FIG. 3C

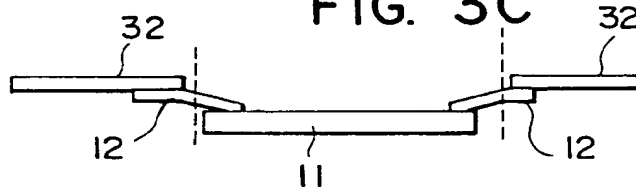


FIG. 3D

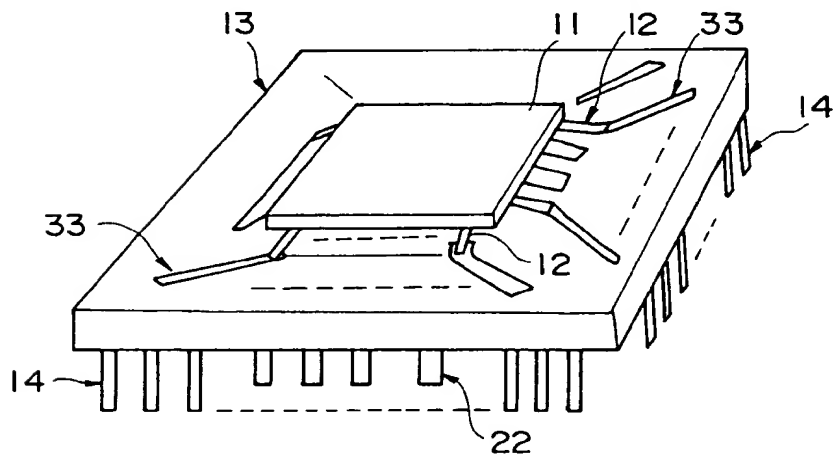


FIG. 3E

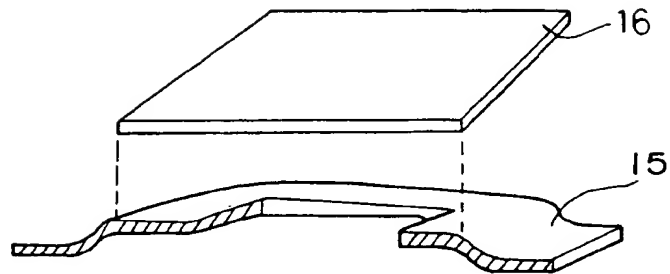


FIG. 3F

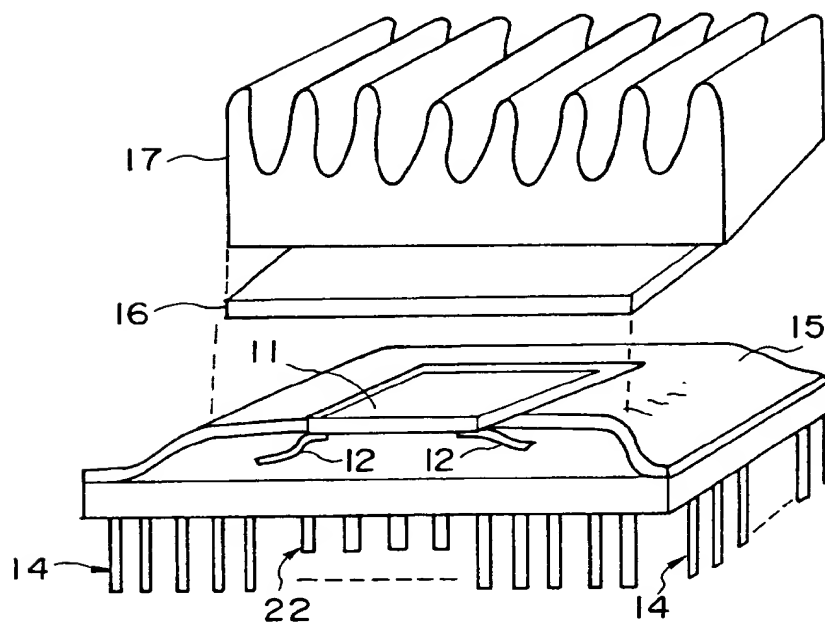


FIG. 4

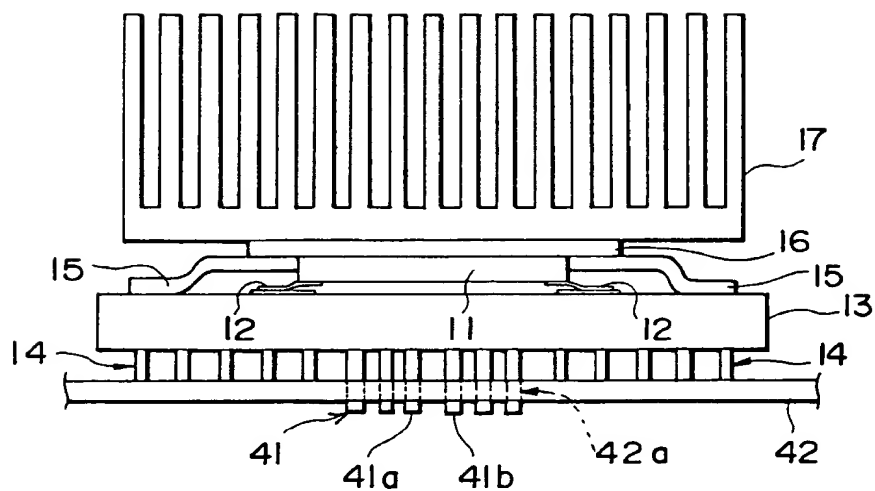


FIG. 5

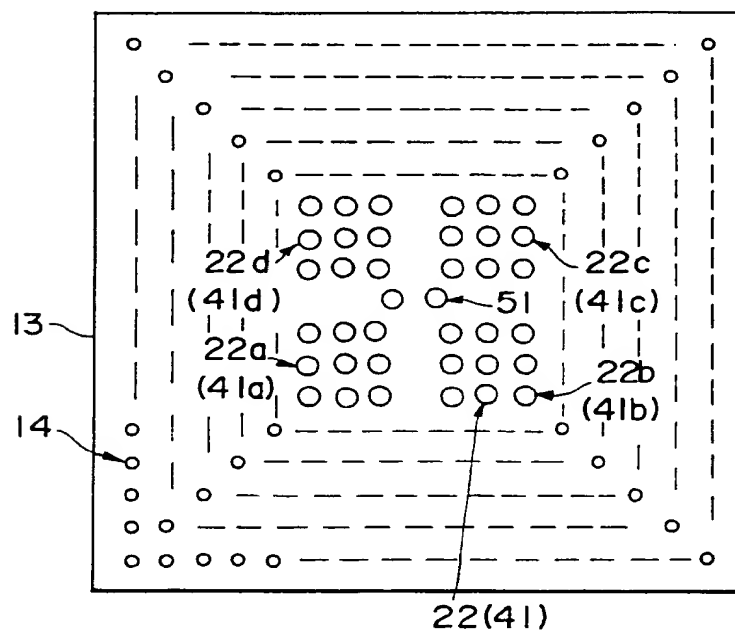


FIG. 6

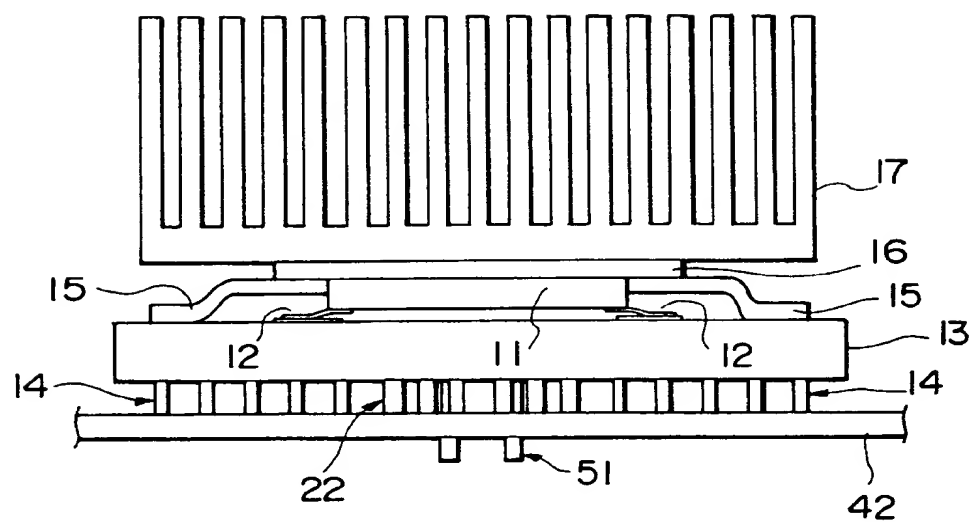


FIG. 7A

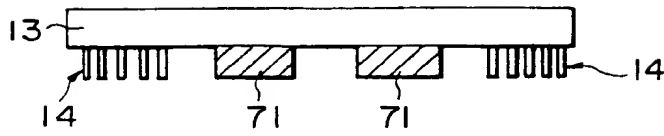


FIG. 7B

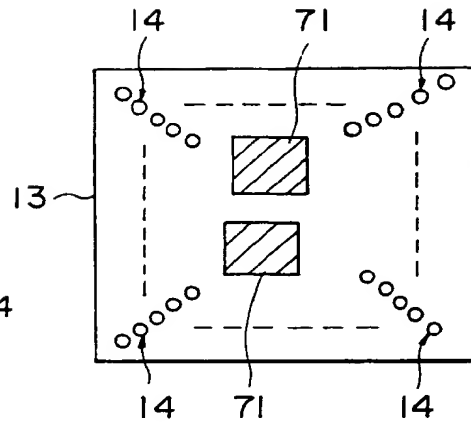


FIG. 8A

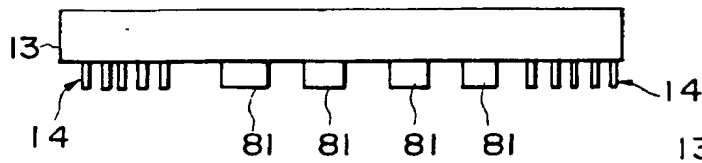


FIG. 8B

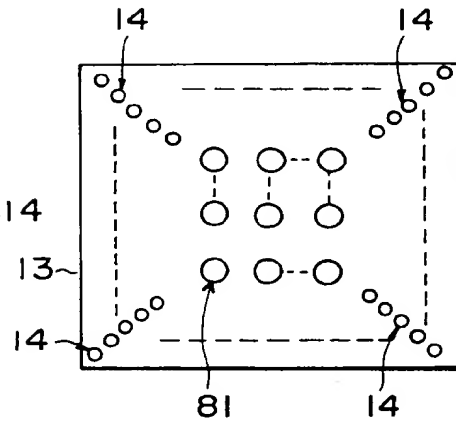


FIG. 9A

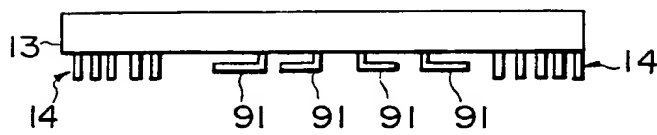


FIG. 9B

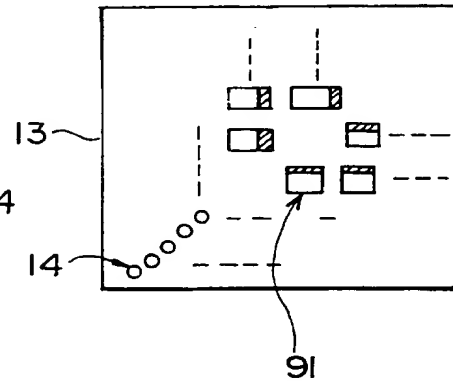


Fig. 10

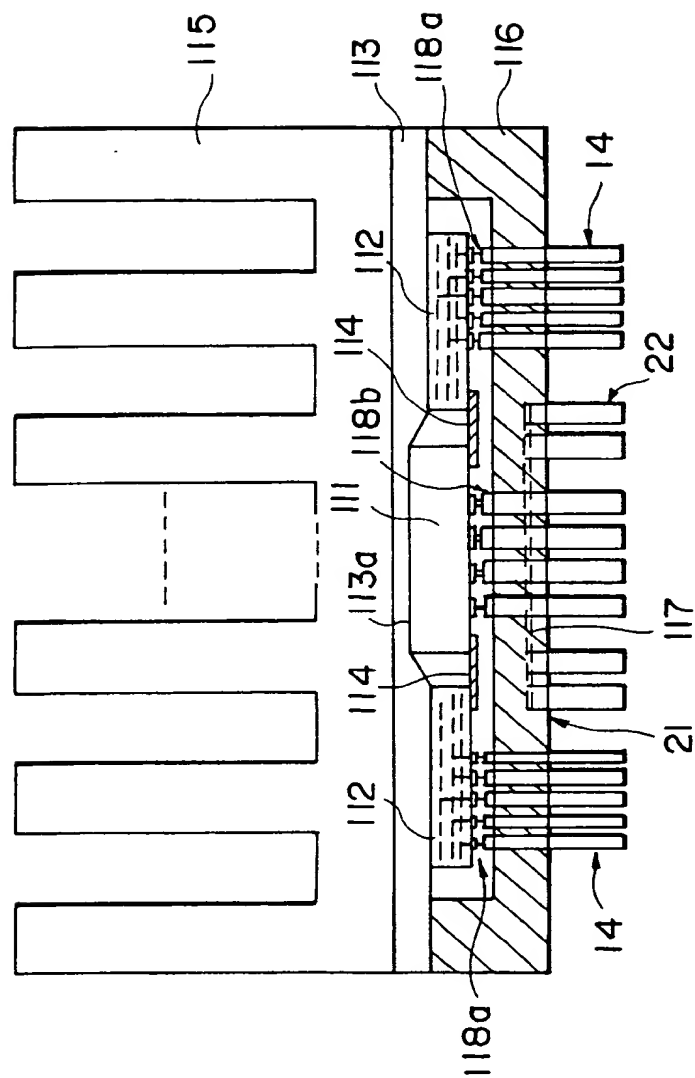


FIG. IIA

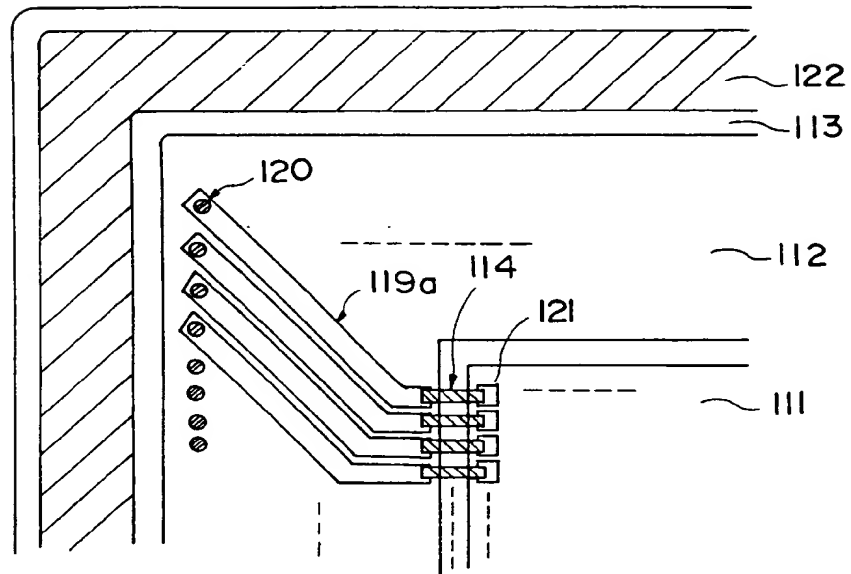


FIG. IIB

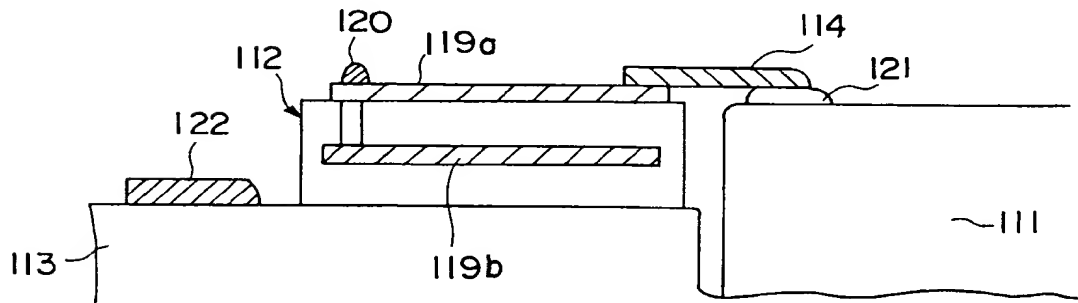


FIG. IIC

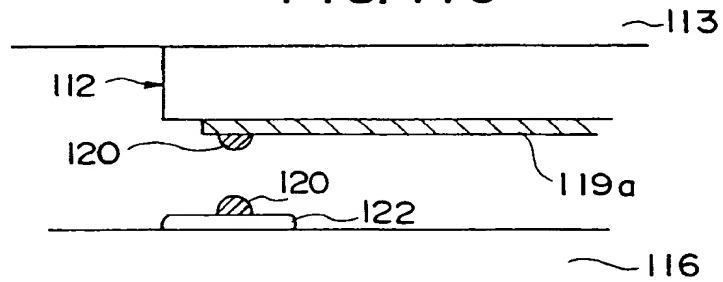


FIG. 12A

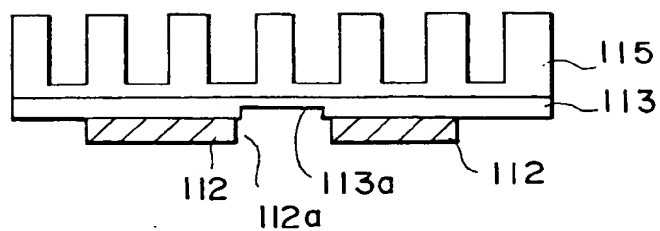


FIG. 12B

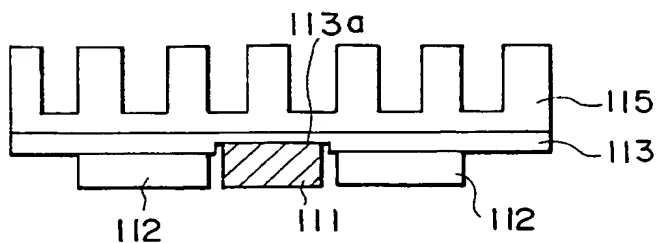


FIG. 12C

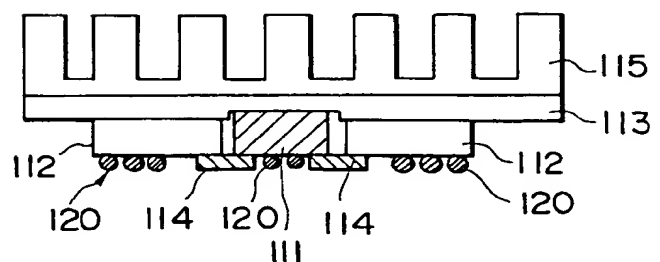


FIG. 12D

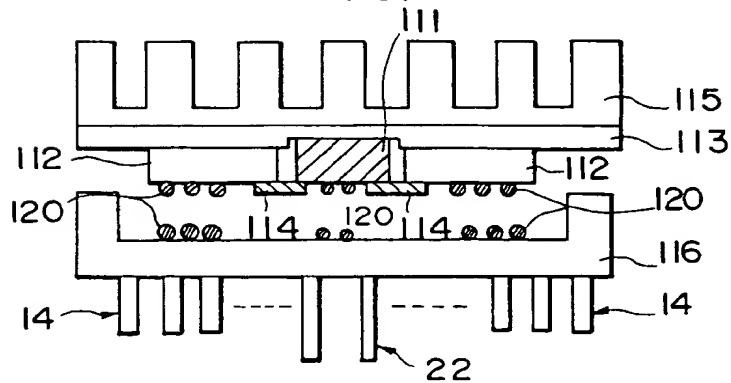


FIG. 13A

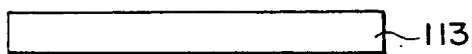


FIG. 13B

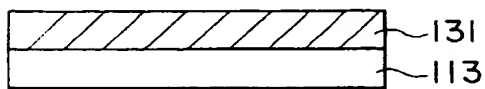


FIG. 13C

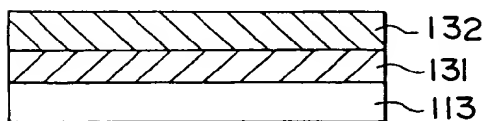


FIG. 13D

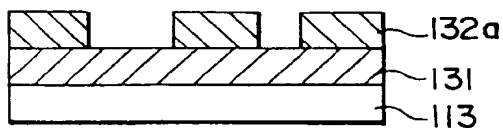


FIG. 13E

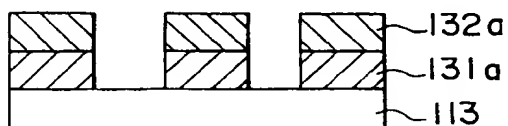


FIG. 13F

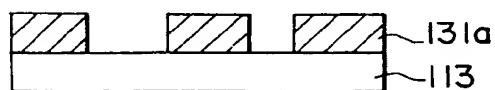


FIG. 13G

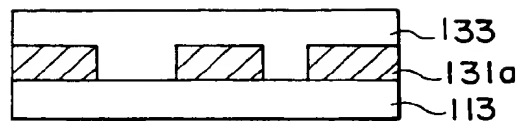


FIG. 13H

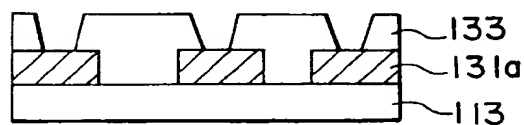


FIG. 13I

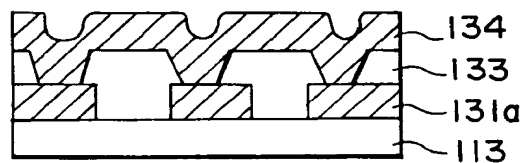


FIG. 14A

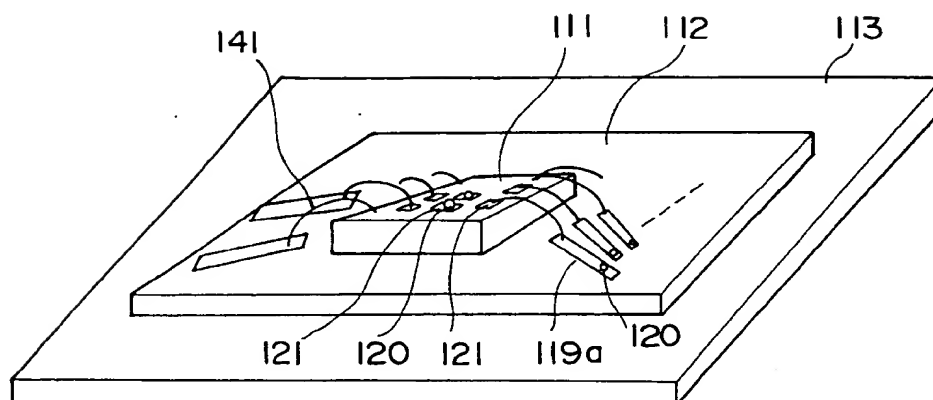


FIG. 14B

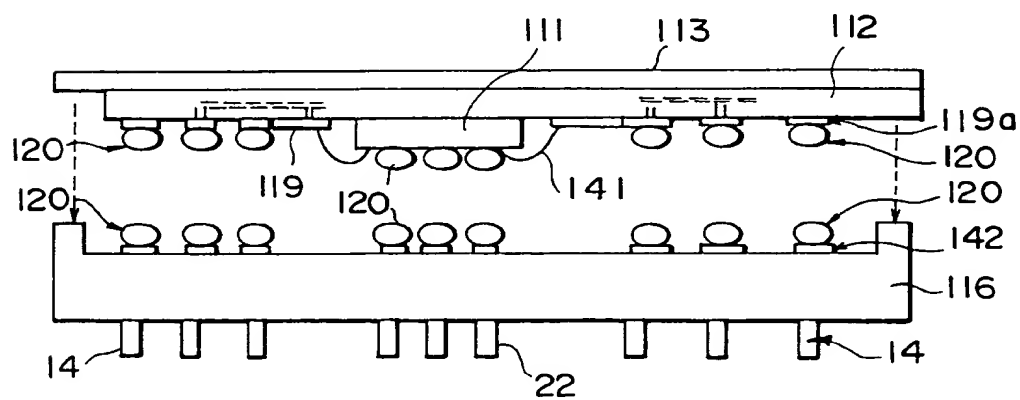


FIG. 15

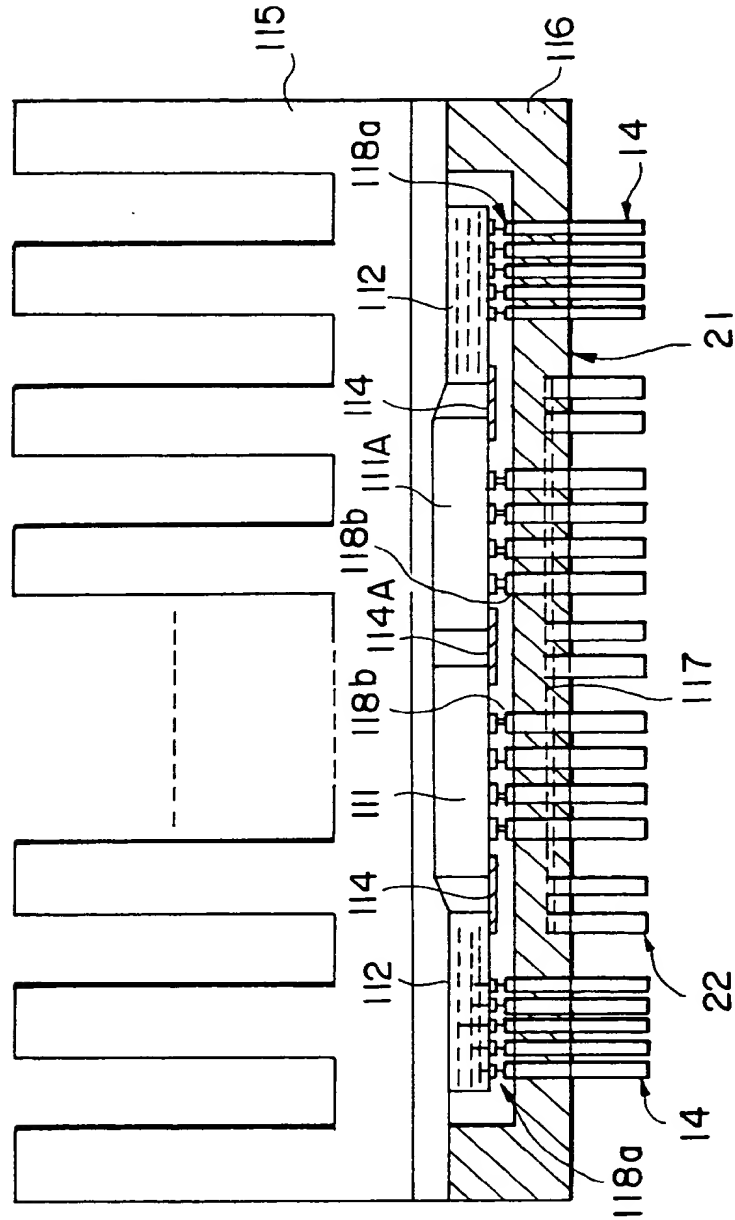


FIG. 16A

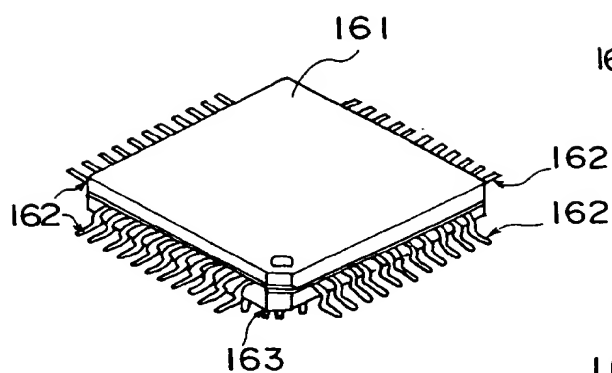


FIG. 16B

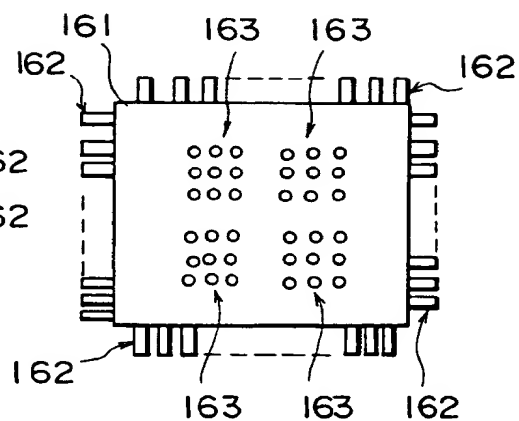


FIG. 17A

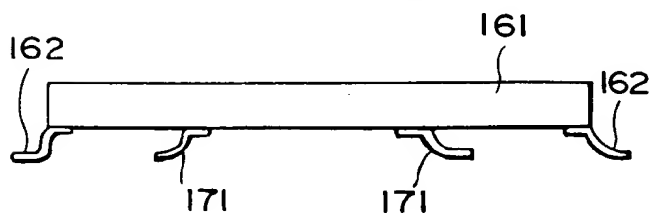
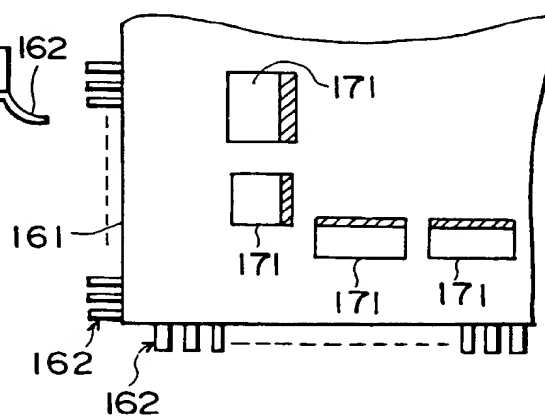


FIG. 17B



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP91/01242

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
Int. Cl ⁵ H01L23/50, H01L23/12		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC	H01L23/50, H01L23/12	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
Jitsuyo Shinan Koho		1926 - 1990
Kokai Jitsuyo Shinan Koho		1971 - 1990
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ¹⁰	Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	JP, A, 2-125650 (NEC Corp.), May 14, 1990 (14. 05. 90), Lines 7 to 9, lower right column, page 2 Figs. 5 to 6 (Family: none)	1
Y	JP, A, 2-125650 (NEC Corp.), May 14, 1990 (14. 05. 90), Lines 7 to 9, lower right column, page 2 Figs. 5 to 6 (Family: none)	2-6, 8-17
X	JP, A, 2-30172 (NEC Corp.), January 31, 1990 (31. 01. 90), Lines 16 to 20, upper right column, page 2 Fig. 1 (Family: none)	7
Y	JP, A, 2-30172 (NEC Corp.), January 31, 1990 (31. 01. 90), Lines 16 to 20, upper right column, page 2 Fig. 1 (Family: none)	6
Y	JP, A, 1-230264 (NEC Corp.), September 13, 1989 (13. 09. 89), Lines 2 to 7, lower right column, page 2	2, 10, 11, 15-17
¹⁰ Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
December 5, 1991 (05. 12. 91)		December 17, 1991 (17. 12. 91)
International Searching Authority		Signature of Authorized Officer
Japanese Patent Office		

Form PCT/ISA/210 (second sheet) (January 1985)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	Fig. 2 (Family: none)	
Y	JP, A, 2-148860 (Hitachi, Ltd.), June 7, 1990 (07. 06. 90), Lines 10 to 18, upper right column, page 5 & EP, A, 371696 & US, A, 4994902	17
Y	JP, A, 1-318251 (Fujitsu Ltd.), December 22, 1989 (22. 12. 89), Line 15, upper right column to line 1, lower left column, page 3, Fig. 1 (Family: none)	3, 4
Y	JP, A, 2-106943 (NEC Corp.),	3

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . . . because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers . . . because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers . . . because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ²

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

April 19, 1990 (19. 04. 90),
Fig. 4 (Family: none)

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers . because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers . because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ²

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
☐ No protest accompanied the payment of additional search fees.